## Part 1: Timing Analysis

### Part 1.1: Determine the Machine Architecture

**1-1 DISCUSSION QUESTION**

Caches in modern processors are generally set-associative. Use the commands above and what you learned in 6.1910[6.004] to fill in the blanks in the following table. The L1 line size has been filled in for you.

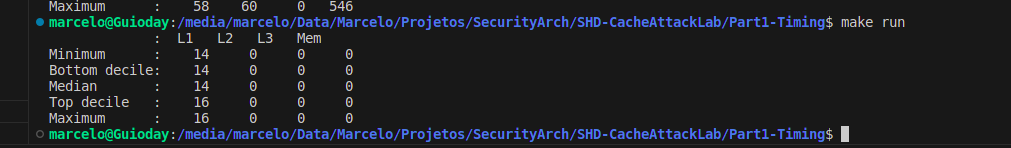
**Rocket Lake - Microarchitectures - Intel - 11th Gen Intel(R) Core(TM) i7-1165G7 @ 2.80GHz**

| **Cache** | **Cache Line Size** | **Total Size** | **Number of Ways (Associativity)** | **Number of Sets** | **Raw Latency** |
| --- | --- | --- | --- | --- | --- |
| L1 | 64 Bytes | 32 KiB x 4 | 8-way set associative | 64 |  |
| L2 | 64 Bytes | 1,2 MiB x 4 | 8-way set associative | 2560 |  |
| L3 | 64 Bytes | 12MiB | 16-way set associative | 12288 |  |

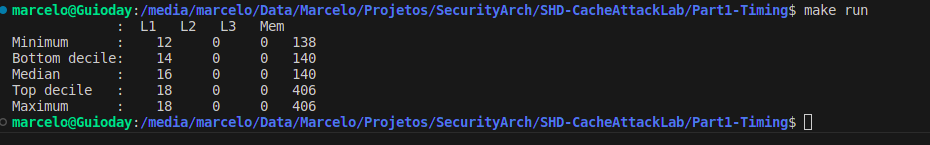
<https://en.wikichip.org/wiki/intel/microarchitectures/rocket_lake>

### Part 1.2: Timing a Memory Access

### Measuring L1 Latency



### Measuring DRAM Latency



### Measuring L2 and L3 Latencies

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